

REMARKS

Claims 3, 4, 6-9, 11-17, 19-26, 55-62, and 75-79 are pending in this application. Claims 6, 8, 9, 11, 12, 15-17, 19-26, 55-62 and 75-78 stand allowed. Applicant acknowledges, with appreciation, the Examiner's indication that claims 3, 4, 7, 13, and 14 would be allowable if the rejection under 35 U.S.C. §112, first paragraph is overcome.

In this Amendment, claims 3, 4, 7, 13, and 14 have been amended, and new claims 80-84 added. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the amendment of claims 3, 4, 7, 13, and 14 can be found in, for example, Figs. 5, 8, 11, and 13 and relevant description of the specification. Adequate descriptive support for new claims 80-84 can be found in Fig. 23 (see clock control register 101) and relevant description of the specification.

Claims 3, 4, 7, 13, and 14 have been rejected under 35 U.S.C. §112, first paragraph.

The Examiner asserted, "the newly added limitations 'the difference between the logic low period and the logic high period of said output clock signal is maintained' and 'maintaining that duty ratio of said output clock signal' are not described in the specification of the instant application" (paragraph 2 of the Office Action).

In response, Applicant has amended the claims for clarification. For example, claim 5 now recites, "the difference between the logic low period and the logic high period of said output clock signal is maintained under a predetermined level of a control signal" (emphasis shows a change). This recitation is clearly supported by Figs. 5, 8, 11, and 13, and relevant description of the specification.

Applicant invites the Examiner's attention, for example, to the second and third full paragraphs of the specification, which are reproduced below (emphasis added):

When driving capability control signals DRVP, DRVN are at H level, L level, respectively (times t1-t2), the output of logical gate 25 is correlated with the change of input buffer signal BIN, whereas the output of AND gate 26 is always at L level. As a result, P-channel MOS transistors 22, 27 both turn on when input buffer signal BIN is at L level, whereas only N-channel MOS transistor 23 turns on and N-channel MOS transistor remains off when input buffer signal BIN is at H level.

Therefore, at times t1-t2, in buffer circuit 10b, the driving capability in inverter 21 is greater on the side of P-channel MOS transistors 22, 27 than the driving capability on the side of N-channel MOS transistors 23, 28. In other words, the delay amount of input buffer signal BIN at inverter 21 is larger during the transition from L level to H level than during the transition from H level to L level. Therefore, output buffer signal BOUT has an L level period TL1 longer than an H level period TH1 at times t1-t2, as shown in Fig. 5.

It is apparent that the above paragraph exemplarily describes that output buffer signal BOUT has an L level period TL1 longer than an H level period TH1, and such difference between the L level period and the H level period is maintained during times t1-t2 based on the levels of control signals DRVP, DRVN. Applicant respectfully requests the Examiner to further review Figs. 8, 11, and 13, and relevant description of the specification. Accordingly, the limitations recited in claims 3, 4, 7, 13, and 14 have adequate descriptive support in the written description of the specification.

Applicant believes that the above discussion is fully responsive to the Examiner's concerns. Withdrawal of the rejection of claims 3, 4, 7, 13, and 14 under 35 U.S.C. §112, first paragraph is, therefore, respectfully solicited.

Since Applicant believes that the rejection of claims 3, 4, 7, 13, and 14 under 35 U.S.C. §112, first paragraph will be overcome, the Examiner's indication that these claims are allowable over Yen, would be maintained (paragraph 5 of the Office Action).

New Claims 80-84

Applicant believes that Yen, the AAPA, and Suda, either individually or in combination, do not disclose or teach all the limitations recited in new claims 80-84. Favorable consideration is, therefore, respectfully solicited.

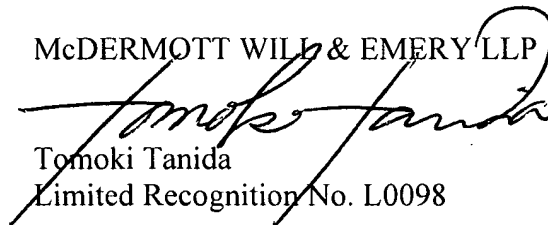
Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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